Polaris LoRa Receiver

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Introduction

The Satlab Polaris LoRa is a fully self-contained software-defined radio receiver for the 865-870 MHz band, with integrated demodulators for reception of SF 8 and 9. This versatile SDR offers excellent performance given the typical size, weight and power constraints of a CubeSat - or as an additional payload on larger LEO satellites.

Features

- Stand-alone LoRa receiver
- Integrated LNA and SAW filters
- Onboard data storage for LoRa frames
- Support for spectrum sample capture
- Safe on-orbit software upgrade support
- CAN-bus, RS-422 and Ethernet interfaces using CubeSat Space Protocol (CSP)
- Delivered with support library for easy integration
- Wide input voltage range with protection
- Integrated temperature and power monitoring
- CubeSat Kit compatible aluminum enclosure
- ESD protection on all interfaces

Key Parameters

Parameter	Specification
Frequency coverage	865.000 to 870.000 MHz
Bandwidth	125.000 kHz
Spreading factors (SF)	8 and 9
Coding rate (CR)	1, 2, 3 and 4
Payload length	2 to 250 B
Sensitivity	-130 dBm (99% reception rate, SF9 with CR4)
Frame store capacity	130000 frames
Input voltage	4.5 to 40 V
Typical power consumption	1.5 W (5 V input, 25℃)
Operating temperature	-40℃ to +85℃
CAN-bus	Up to 1 Mbit/s
RS-422	Full duplex, up to 3 Mbit/s
Ethernet	Full duplex, 100 Mbit/s
Primary storage	128 MB NOR-flash
Secondary storage	1 GB SLC SD card
Dimensions	93.0 x 87.2 x 12.5 mm
Mass	185 g

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1 Description

The Satlab Polaris LoRa is a fully self-contained software-defined radio receiver for the 865-870 MHz band, with integrated demodulators for reception of SF 8 and 9. This versatile SDR offers excellent performance given the typical size, weight and power constraints of a CubeSat - or as an additional payload on larger LEO satellites. The receiver is designed to decode large messages under high Doppler rates (500 Hz/s) without performance degradation.

The receiver uses a high-performance, direct-conversion front end and large dynamic range ADC to receive the 865-870 MHz band. Digital filtering and down conversion is used to extract and demodulate the SF 8 and 9 frames in parallel. The board features on-board low noise figure LNA and SAW filters and only requires a passive antenna for reception.

The demodulation algorithm uses per-frame sampling offset and center frequency estimation, which ensures good reception even for weak messages at large Doppler frequency offsets. Demodulators and wideband processing modules can safely be upgraded on-orbit, e.g. to test improved receiver algorithms or to add additional LoRa channels after launch.

On-board data storage simplifies integration, allowing received LoRa messages to be queried directly from the receiver without intervention from the spacecraft OBC. The receiver can also be operated in a receive-and-forward mode if an external message store is preferred.

Figure 1 shows the Polaris LoRa with external interfaces to the satellite bus and receiving antenna.

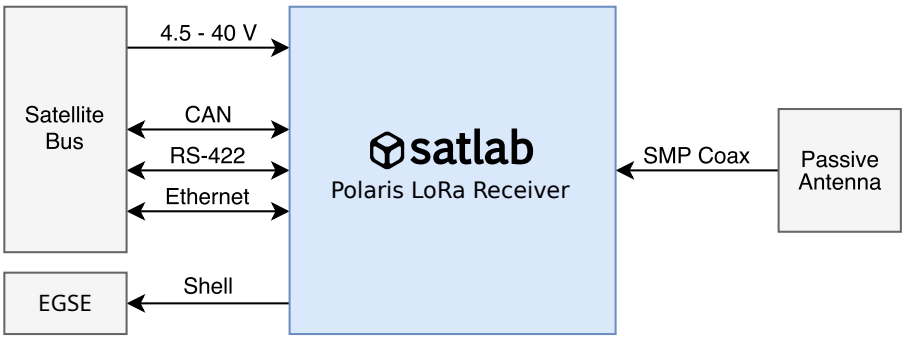


Figure 1: Overview of the Satlab Polaris subsystem external interfaces

Polaris LoRa is powered from a single 4.5 to 40 V input voltage and is compliant with ECSS-E-ST-20-20C, 28 V unregulated power supplies. The power input and all onboard regulated voltages are protected against over-current.

The receiver is delivered in a milled aluminium enclosure which provides a strong mechanical interface as well as EMI shielding and thermal contact. The main and EGSE connectors are latching, high-reliability Harwin Gecko connectors with gold plated contacts. A full detent Amphenol coaxial SMP connector is used for the antenna input.

The board is operated via CAN-bus, RS-422 or Ethernet using Cubesat Space Protocol[1] (CSP) commands. Multiple communication interfaces can be enabled simultaneously and serve as backup. Satlab supplies client libraries in C and Python to wrap the CSP protocol, along with example code to simplify integration even further.

A serial command line shell is available through the EGSE connector, which can be used for on-ground configuration, testing and performance verification.

[1] See `http://www.libcsp.org` for documentation on the open source reference implementation.

2 Receiver Performance

The typical receiver packet error rate (PER) versus input signal power is illustrated on figure 2. The test is performed with 10 bytes packets, CRC enabled and CR 4 at 0 Hz frequency offset.

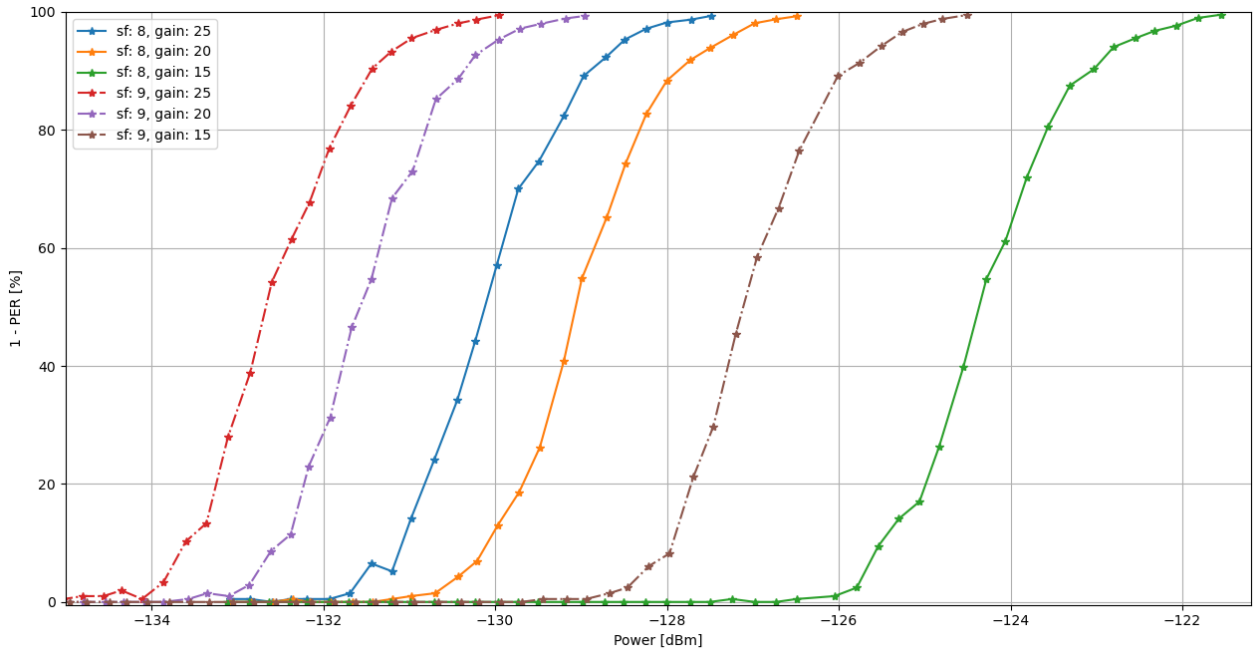


Figure 2: Typical receiver packet error rate for receiver gain 20 and with 0 Hz frequency offset and CR 4

A summary of the sensitivity is shown in table 1.

Table 1: Receiver input power in dBm for PER <10 % and PER <1 % @ 869.525 MHz (25℃)

SF	Gain setting	Power [dBm] @ PER <10 %	Power [dBm] @ PER <1 %
SF8	25	-128.9	-127.6
SF8	20	-127.8	-126.6
SF8	15	-123.0	-121.8
SF9	25	-131.4	-130.1
SF9	20	-130.3	-129.1
SF9	15	-125.9	-124.7

In figure 3 the typical measured reception performance for the LoRa demodulator is shown for SF 8 and 9 at room temperature with each frames sent at a random frequency in the interval -25 kHz to 25 kHz from the nominal center frequency.

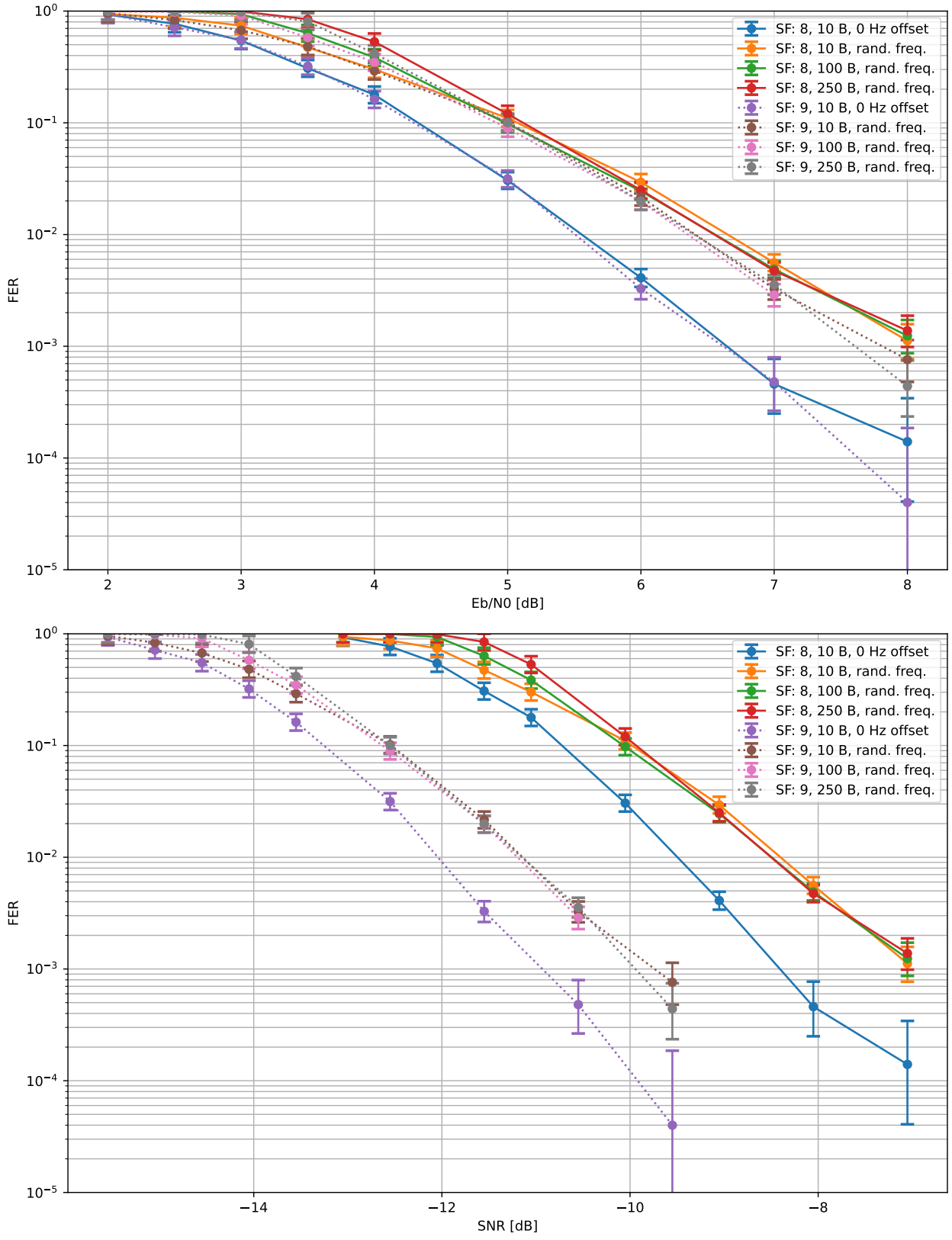


Figure 3: Typical demodulator performance for SF 8 and 9 as a function of Eb/N0 and SNR for different frame lengths. Test done on hardware with high enough input that receiver noise figure can be ignored. LoRa frames sent with random frequency offset between -25 kHz and 25 kHz. One SF 8 and one SF 9 test done with frequency offset of 0 Hz to show the difference in performance.

3 Hardware Overview

This section provides a high-level overview of the Polaris LoRa platform hardware, with descriptions of the RF front end, baseband processing system, power domains and telemetry.

3.1 RF Front End

The receiver uses a direct-conversion, low-IF quadrature front end in conjunction with a 16-bit, 25 Msps dual channel ADC. Figure 4 shows the main receiver hardware components. Buffers and ADC drivers are not shown for simplicity.

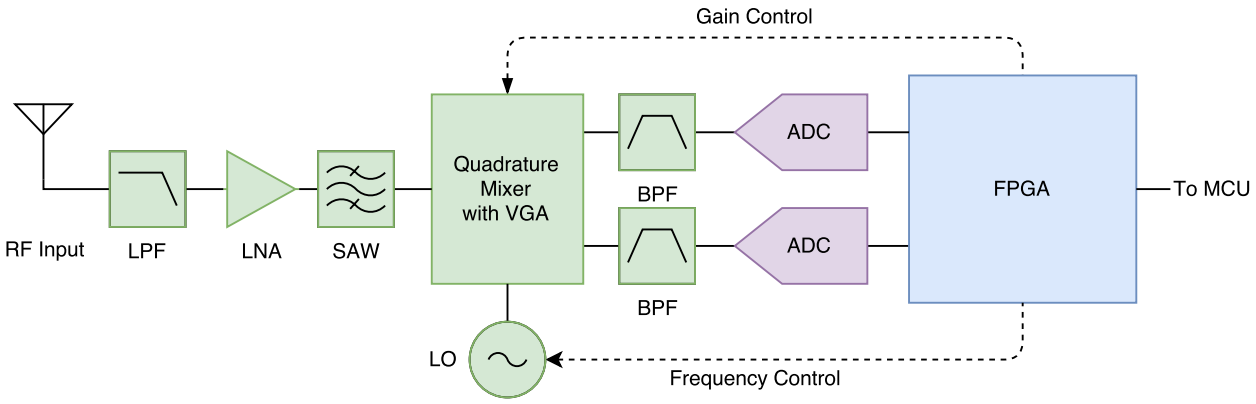


Figure 4: Overview of the RF hardware structure

The receiver requires a single 865-870 MHz antenna connected to the RF connector. The Low Pass Filter (LPF) reduces the influence of strong nearby transmitters, such as satellite downlink in the UHF- and S-band.

The on-board LNA ensures a good noise figure for the overall system, and simplifies the final integration process as the system only requires a passive antenna.

Out-of-band rejection is ensured both by the on-board SAW filter and the IF band pass filters.The VCO is internally divided in the mixer to generate an upper-side LO, significantly reducing any LO leakage.

The quadrature mixer has a built-in VGA with adjustable gain that can be set via telecommands.

The FPGA converts the wideband complex input stream into one filtered baseband output stream. Internally the FPGA uses multiple filtering and decimation stages to maintain the dynamic range needed when receiving from many different transmitters at the same time.

3.2 Baseband Processing

The MCU receives channelized data from the FPGA and demodulates the LoRa data frames and connects to data storage and communication interfaces. Figure 5 shows the MCU and connected peripheral devices.

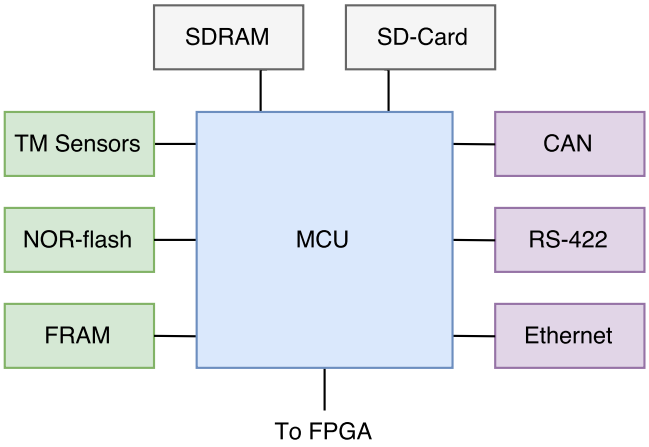


Figure 5: Overview of the MCU with data storage and communication interfaces

A 128 MB NOR-flash is used as the primary storage for received LoRa frames. A 1 GB SD card is used as secondary storage for raw samples, software uploads and snapshots of the LoRa store. The FRAM is used to store non-volatile configuration parameters such as CSP address and communication interface settings. CAN-bus at 1 Mbit/s is the default interface. RS-422 and Ethernet is not used by default, but these interfaces can be enabled permanently or by command, e.g. when the spacecraft is within range of a high speed ground link.

The board contains an external 64 MB SDRAM which is disabled by default to limit power consumption, and not required for normal LoRa reception on the device. The external memory is used when capturing raw samples, and is automatically enabled on sample requests.

Temperature and power sensors for telemetry are connected on a dedicated telemetry bus.

The MCU and FPGA are connected using a unidirectional serial link for multiplexed data transfer and a bidirectional SPI bus for configuration.

3.3 Power Domains and Telemetry

Figure 6 shows a simplified diagram of the power domains, protection and monitoring of the device. The input protection circuitry guards the board against over-voltage and reverse-voltage conditions, and performs active inrush current limiting and over-current protection. Refer to the Electrical Specifications section for the protection limits and recommended operating conditions. The external watchdog/reset timer is powered from V_{IN} with a current-limiting 3.3 V LDO and resets the main regulator on system power-on or in case of watchdog timeout. This ensures that all components on the board are reset to a known state when the system boots.

During power-on of the device, the inrush current is limited only by the voltage slope and the input capacitance of 1μF in series with a 1Ω resistor. In this moment the spacecraft Power Distribution Unit (PDU) or Electronic Power Supply (EPS) is responsible for keeping current spikes at a reasonable level. Once the input voltage is above the minimum threshold (max 4.5 V) the internal protection circuit is enabled and active current limitation of 2 A is used during system power on and operation. The protection reset timer of 420 ms actively discharge internal power nets before powering the MCU and FPGA using a strictly defined startup sequence.

The main buck converter converts V_{IN} to 3.3 V which powers the MCU and FPGA I/O, and the 2.0 and 1.0 V converters. Power for the MCU core, ADC and FPGA I/O is generated using LDOs from the 2.0 V rail. The MCU control the power for the RF, FPGA and ADC domains using GPIOs.

The SD card and Ethernet PHY are powered off by default and must be powered on by the MCU. Both load switches are current limiting.

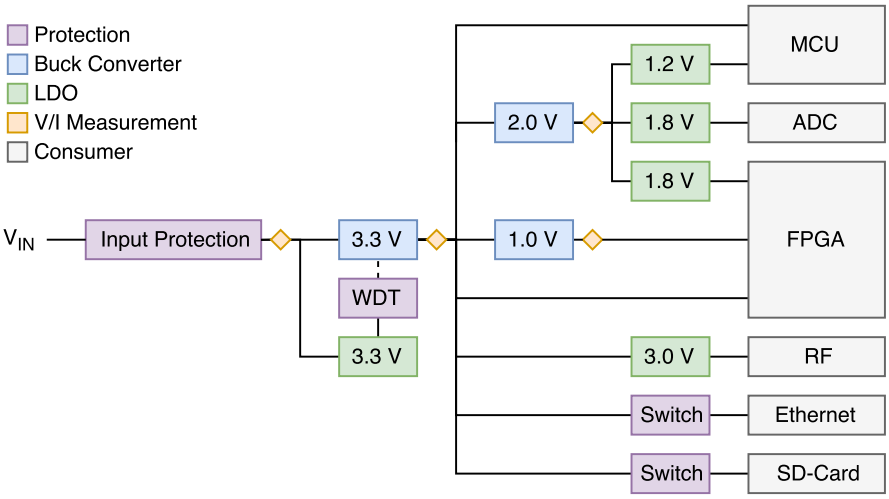


Figure 6: Power domains and protection circuitry

Each local power domain of the receiver features over current protection for error mitigation purpose, to reduce the impact of any Single Event Latchup (SEL) events. Voltage, current and power can be measured on the V_{IN}, 3.3, 2.0 and 1.0 V rails and can be downloaded using telemetry properties. The measurement points are marked in figure 6 with yellow diamonds. Note that the V_{IN} sensor is placed after the input protection circuitry, which has a equivalent series resistance of approximately 140 mΩ, so the measured voltage and power are lower due to the corresponding voltage drop. It should also be noted that the 1.0 and 2.0 V supplies are generated from the 3.3 V rail, so the 3.3 V power measurement includes the power used by the two other rails.

The board has seven temperature measurement points, located on-die or near key components on the PCB. The temperature and power sensors are listed in table 2 along with their telemetry property name.

Table 2: Onboard telemetry sensors

Property	Description
`tm.{volt,cur,power}.vin`	V_{IN} voltage, current and power
`tm.{volt,cur,power}.3v3`	$V_{3.3V}$ voltage, current and power
`tm.{volt,cur,power}.2v0`	$V_{2.0V}$ voltage, current and power
`tm.{volt,cur,power}.1v0`	$V_{1.0V}$ voltage, current and power
`tm.temp.mcu`	MCU, SDRAM and NOR-flash temperatures
`tm.temp.fpga`	FPGA junction temperature
`tm.temp.power`	1.0/2.0 V buck converters temperature
`tm.temp.lna`	LNA and front end components
`tm.temp.adc`	ADC temperature
`tm.temp.sdcard`	SD card temperature

4 Software Overview

Figure 7 shows the main software components and data flow in the Polaris LoRa receiver. The software can be grouped in two main parts: the bitstream for the FPGA and firmware for the MCU. This section describes the operation of each component.

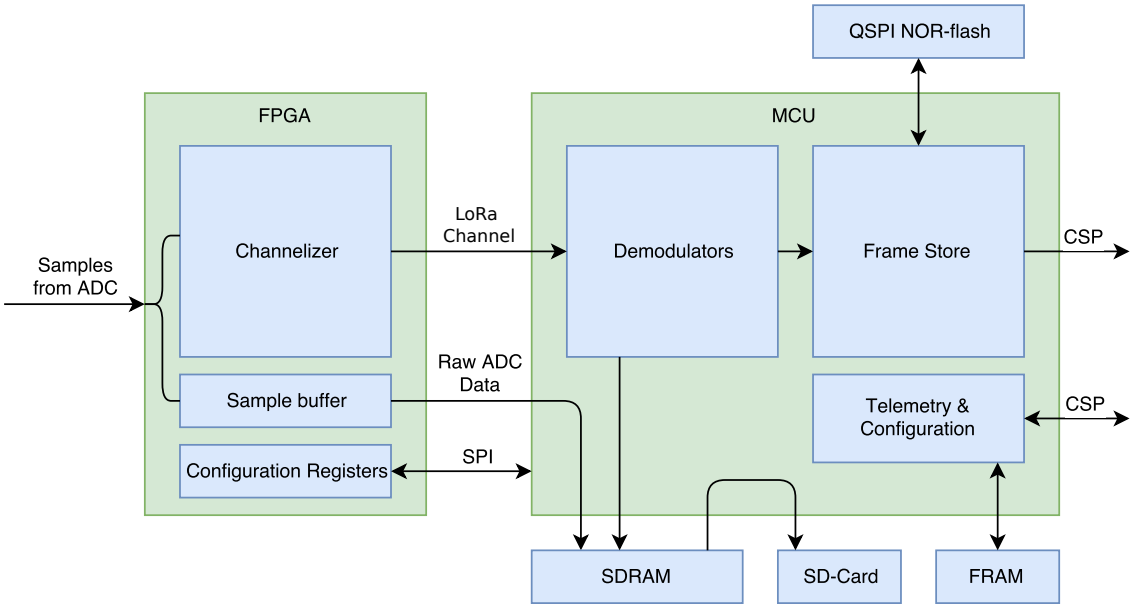


Figure 7: Overview of the receiver software components

The system always boots from internal NOR-flash on the MCU with the RF components and FPGA powered down. The flash sectors are divided into two equally sized image partitions: A primary image which is programmed and locked at production time and can only be updated using JTAG/SWD through the EGSE connector, and a secondary image that can be flashed by the board itself and upgraded on-orbit.

On system startup the receiver selects between the two firmware images by checking a special section in FRAM. New receiver firmware can be uploaded to the SD card via CSP. Once the firmware is fully uploaded and verified, it can be programmed to internal flash and marked for boot a specified number of times. Firmware images contain both the main application and the matching embedded FPGA bitstream, allowing synchronized on-orbit update of both.

The receiver is operated remotely using CSP commands via one of the external communication interfaces.

4.1 FPGA Bitstream

The FPGA is automatically powered on and loaded by the MCU during startup of the LoRa demodulators. The bitstream contains a channelizer to convert the 25 Msps ADC input stream to one filtered, 500 ksps, complex baseband output stream. The channelized data is sent to the MCU via a multiplexed serial link.

The bitstream also implements a small internal sample buffer with a capacity of 8192 complex 16-bit samples, i.e. approximately 327 µs at 25 Msps. A capture to the buffer can be triggered via CSP command and the data downloaded from either SDRAM or the SD card. Because of the short capture length, this feature is mainly useful to check for interferers in the full spectrum data, on ground or after launch. Much longer captures of the filtered LoRa channel is possible using the capture interface through the MCU.

An SPI slave controller is also included in the FPGA image, which provides access to various internal configuration and status registers.

4.2 MCU Firmware

The MCU firmware implements a real-time operating system, device drivers for internal and external peripherals, LoRa demodulators, frame storage and CSP servers for telecommands and telemetry.

4.2.1 Demodulator and Frame Decoder

The demodulator and frame decoder are responsible for converting the sampled data to valid LoRa frames. The channelized sample stream from the FPGA is processed using parallel demodulator chains, one for each spreading factor. Figure 8 outlines the data processing steps in each chain.

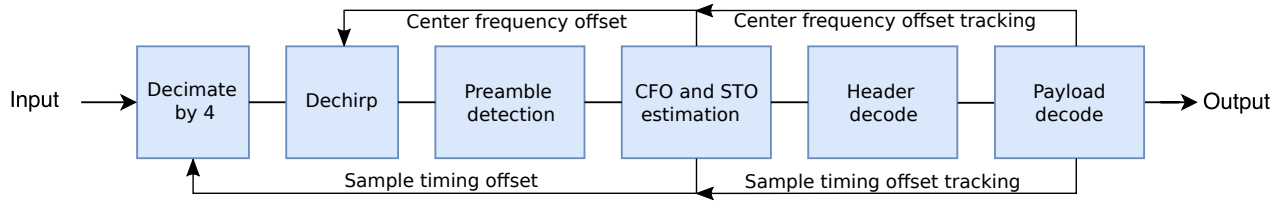


Figure 8: Overview of the demodulator and frame decoder processing steps

Preamble detectors are run on the filtered data to search for possible frames on the channel. Key signal parameters are estimated for each individual LoRa frame, and used to ensure good reception in LEO.

When a frame is detected the receiver estimates the center frequency offset and sample timing offset. With the center frequency and sample timing corrected the header of the LoRa frame can be decoded. The header contains information about the coding rate and length of the payload part of the LoRa frame so a valid header is need to proceed to the payload decode step. After the payload has been decoded a CRC check is performed and if it passes the payload data is passed to the frame store queue.

Various configuration parameters, such as frame detection counters for the demodulators, are available through configuration and telemetry parameters. Using the `demod.enable` boolean property it is possible to enable or disable the demodulation temporarily.

A special operating mode allows the MCU to save raw channelized samples to external SDRAM or the SD card, for download and processing on ground. The default sample format is uncompressed, 16-bit quadrature samples at 250 ksps, and the maximum sample length is only limited by the 64 MB SDRAM to approximately 64 seconds. Triggering a raw sample does not disable demodulation while sampling.

4.2.2 Message Store

Each received message is tagged with a 32-bit sequence number and stored in NOR-flash with reception metadata (estimated center frequency offset, signal level) and a 64-bit timestamp (number of nanoseconds since midnight on January 1st, 1970). All SF 8 and 9 frames are stored in the same store, and consumes 512 bytes of NOR flash, including metadata, independent on the number of payload bytes in the frame. The store is a ring buffer and wraps around every 130560 frames.

Frames can be selectively downloaded by their sequence number through the store CSP service, and provides access to the full LoRa payload and metadata. The entire store can also be dumped as a binary file to the SD card for more efficient download. It is of course possible to clear all stored data.

4.2.3 CSP Services

Three CSP servers are used to configure the receiver, read back status and to download messages and raw samples. File transfer is handled using the Blob Transfer Protocol (BTP), a lightweight file transfer protocol built on CSP that is

used to provide reliable transfer of raw sample files and firmware images.

4.2.4 EGSE Console

The system provides a serial console on the RX/TX pins in the EGSE connector (see section 6.3). The serial configuration is 8N1 at 115200 baud, and the console requires an ”Enter” key press to be activated.

Listing 4.1 shows the nominal output on the serial console during boot. A number of timestamped log messages are printed during boot from various logging groups. Additional logging can be enabled at runtime using the `trace` commands. The `help` command can be used to list available commands and their usage.

The installed software version and build information is also printed in the console during boot.

Listing 4.1: Example output from console

```
[    0.000702] prop: using stored sys properties
[    0.000904] prop: using stored demod properties
[    0.001078] prop: using stored store properties
[    0.001224] system: Copyright (c) 2016-2023 Satlab A/S <satlab@satlab.com>
[    0.008259] system: boot: 566342 reset cause: general reset
[    0.016234] system: board serial #2226ce86

Satlab Polaris LoRa v1.0.0

[lora] help
Available commands:
boot            Bootloader commands
csp             CSP commands
echo            Display a line of text
fs              File system commands
help            Show available commands
history         Show previous commands
prop            System configuration properties
reboot          Reboot system
store           Frame store commands
time            Time command execution
tm              Telemetry commands
trace           Trace subcommands
uptime          Show system uptime
watch           Run command periodically
```

4.3 Configuration & Telemetry

Configuration, status and telemetry download from the device is handled using a number of property variables. Each variable has a type (signed/unsigned integers of various sizes, floating point numbers, strings, etc.) and a default value. Some properties are used for configuration and can be modified and stored in (optionally write-protected) non-volatile memory using the console or remotely via CSP commands. Others are read-only and used for telemetry purposes. These properties are periodically updated by the system during operation, and can also be viewed using either the console or via CSP.

Some property changes take effect immediately, while others require a store and a system reset after update.

The system properties are divided into a number of property groups, each covering a specific part of the firmware. Property values can be read and updated from a remote system using CSP. The `prop-client` support library contains wrapper functions around the CSP protocol to read and update properties. The `satctl` Linux application can be used as a reference for the use of the library.

4.3.1 Configuration

On boot, the system tries to load stored properties from FRAM. Default settings are hardcoded into the receiver firmware and used as fallback values if no valid stored properties are found.

It is possible to change properties runtime without saving them to FRAM. It is strongly recommended not to alter write-protected properties on-orbit (e.g. CSP address), since setting them to a invalid value could render the receiver unresponsive.

Listing 4.2 shows the use of the `prop list` command to show properties and their values from the `store` and `demod` groups.

Listing 4.2: List properties and values from the `store` and `demod` groups

```
[lora] prop list store
Property         Type       Value
enable           bool       true
seq              u32        1381198
stored           u32        260984 frames
[...]
[lora] prop list demod
Property         Type       Value
enable           bool       true
decoded          u32        3817
detected         u32        4436
freq             u32        869525000 Hz
rf.gain          float      20.000000 dB
ttrack           bool       true
ftrack           bool       true
[...]
```

4.3.2 Telemetry

The property system is also used to read the telemetry variables from the Polaris LoRa receiver. Telemetry values are updated every second and are available through the `tm` property group. The example below shows the use of the `tm show` shell command which uses the property system to read and output formatted telemetry values. In the example, the board is connected to a 5.0 V bench supply without sense connection. The average board temperature seems to be around 33.2 ℃ with the FPGA junction temperature at 35.18 ℃.

Listing 4.3: List telemetry properties and values

```
[lora] tm show
Power Channels
FPGA           On
RF             On
SD-card        Off
Ethernet       Off

Power Rails
VIN        4925.00 mV    246.00 mA   1198.00 mW
3V3        3336.00 mV    348.00 mA   1165.00 mW
2V0        2000.00 mV    216.00 mA    433.00 mW
1V0         957.00 mV     78.00 mA     74.00 mW

Temperature Sensors
MCU          33.00 C
FPGA core    35.18 C
Power        32.18 C
LNA          33.06 C
ADC          33.37 C
SD-card      32.43 C
```


5 Qualification

The Polaris LoRa receiver has been through a number of test campaigns to verify its performance over temperature, vacuum, vibration and radiation. An overview of the testing performed on the receiver is shown in table 3. As this list is non-exhaustive, please contact Satlab for further information if needed.

Table 3: Qualification Parameters

Parameter	Value
Thermal soak	-40℃ to +85℃
Vibration	14.1 G_{rms}
TID	20 kRad(Si) board level

It should be noted that the levels which are listed in table 3 is a superset of the different tests the receiver has been through during various test campaigns.

The base polaris hardware platform has extensive flight heritage and the Polaris LoRa variant was first tested in space 2022 Q2.

6 Electrical Specifications

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25℃ and V_{IN}= 5.0 V, by production test and/or design characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature.

6.1 Absolute Maximum Ratings

The table below lists the minimum and maximum allowable levels on the connector pins. Exceeding these may damage the product permanently.

Table 4: Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-40	85	℃
Input Voltage	-47	47	V
Input Voltage Transient ($<$5ms)	-60	60	V
RF input power	–	+10	dBm
CAN-L/H	-7	12	V
RS-422	-7	12	V
Ethernet	-0.5	5	V
EGSE-UART (TTL)	-0.5	5	V

6.2 Operating Conditions

6.2.1 General Operating Conditions

Table 5: General Operation Condition

Parameter	Min	Typ	Max	Unit
Operational Temperature	-40	–	85	℃
Input Voltage	4.5	–	40	V
Input current (5.0 V and 25℃)	–	0.29	–	A
Input power (5.0 V and 25℃)	–	1.5	–	W
Input power variation over temperature (5.0 V)	–	1.97	–	mW/℃
Input power variation over supply voltage (25℃)	–	12.17	–	mW/V
Power-on threshold, V_{IN} rising	–	4.35	–	V
Power-off threshold, V_{IN} falling	–	4.15	–	V
OVP threshold, V_{IN} rising	–	43.35	–	V
OVP threshold, V_{IN} falling	–	41.05	–	V

6.2.2 Internal Power Specification

Table 6: Internal Power Specification

Parameter	Min	Typ	Max	Unit
$V_{3.3V}$ rail voltage	3.20	3.33	3.45	V
$V_{2.0V}$ rail voltage	1.90	2.00	2.10	V
$V_{1.0V}$ rail voltage	0.92	0.96	0.98	V

6.2.3 Receiver Specification

Table 7: Receiver Specification

Parameter	Min	Typ	Max	Unit
Variable Gain Array setting range	-18	0	28	dB
Variable Gain Array step size	–	0.1	–	dB

6.2.4 Communication Interfaces

Table 8: Communication Interface Specification

Parameter	Min	Typ	Max	Unit
CAN-bus:				
Termination resistor	115	120	125	Ω
CAN-L/H	-2	–	7	V
CAN-L/H rescessive level	–	2.3	–	V
CAN-L output dominant level	0.5	–	1.3	V
CAN-H output dominant level	2.4	–	3.35	V
CAN dominant L/H difference	1.1	2.0	3.0	V
RS-422:				
Receive termination resistor	–	100	–	Ω
RS-422 RX differential level |Rx+ - Rx-|	0.15	–	6.0	V
RS-422 TX differential output	1.2	2.0	3.5	V
Ethernet:				
ETH-TX Out diff. across 100 Ω termination (Assumes 1:1 transformer)	0.8	1.0	1.2	V
EGSE-UART (TTL):				
TX output high	2.3	3.3	3.4	V
TX output low	0.0	–	0.5	V
RX input low	0.0	–	1.2	V
RX input High	1.9	–	4.0	V

6.2.5 Power-on Sequence and Inrush Current

Table 9: Power ON Sequence

Parameter	Min	Typ	Max	Unit
Power on reset timer	330	420	500	ms
V_{IN} input equivalent at power-on (in series with 1Ω resistor)	0.8	1.0	1.2	µF
Inrush current limiter	1.5	2.0	2.5	A
Current protection limit (3.3V buck)	1.1	1.25	1.4	A

6.2.6 Current Consumption

Table 10: Current/power consumption at 25℃

Parameter	Min	Typ	Max	Unit
VIN 5V, CAN on, Ethernet off, RS-422 off:				
Current	–	270	300	mA
Power	–	1350	1500	mW
VIN 28V, CAN on, Ethernet off, RS-422 off:				
Current	–	58	64	mA
Power	–	1625	1800	mW
Additional power for enabled features:				
Add for SDRAM enabled	–	80	–	mW
Add for Ethernet enabled	–	185	–	mW
Add for RS-422 enabled	–	110	–	mW

6.3 Connector Pinout

P1 and P2 are latching, high-reliability Harwin Gecko connectors with 1.25 mm pitch and gold plated phosphor bronze pins. P1 (G125-MH11605L3P) is the main connector for power and communication interfaces. P2 (G125-MH10605L3P) is used for the EGSE console and programming via SWD. Typically, the P2 connector is only used for test and firmware upgrade on ground and left unconnected in flight configuration. The EGSE UART can be connected to another system in the spacecraft if desired, as the board includes protection against being supplied from these pins. It is strongly recommended to leave the JTAG/SWD pins unconnected in flight configuration.

The Polaris receiver is supplied with termination resistors on the CAN-bus (120 Ω) and on the RS-422 receive pair (100 Ω). The Ethernet connection is designed to be used in systems both with and without magnetics. When using magnetic-less Ethernet a set of external DC blocking capacitors must be used (not included on the board).

The coaxial RF connector is a full detent SMP male connector complient with MIL-STD 348A.

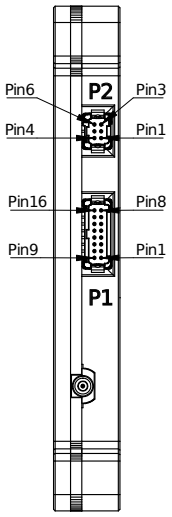
The P1 and P2 connector pinout is shown here together with the pin numbering of the male connectors. ”TX” pins denote output pins from the system and ”RX” pins are inputs to the system.

ESD suppression with TVS diodes has been added to all pins in the three connectors. However, proper care should still be observed while handling the device.

P2 - SWD/Serial EGSE connector			
EGSE TX	6	3	SWDCLK
V_{Target} (sense)	5	2	GND
EGSE RX	4	1	SWDIO

P1 - Main Connector			
VIN	16	8	VIN
DNC	15	7	DNC
GND	14	6	GND
RS-422 RX-	13	5	RS-422 RX+
RS-422 TX-	12	4	RS-422 TX+
CAN-L	11	3	CAN-H
ETH RX-	10	2	ETH RX+
ETH TX-	9	1	ETH TX+

DNC = Do Not Connect



ATTENTION: Although all external interfaces on the Polaris LoRa are protected against ESD, proper precautions must still be observed when handling the device. Ensure proper grounding, either through an antistatic wrist strap and/or floor mat.

7 Mechanical Specifications

Figure 9 shows the receiver from the top side and from the connector side. Note that the four mounting holes use the ”CubeSat Kit” (PC/104) layout and are not symmetrical. CAD models are available on the Satlab website.

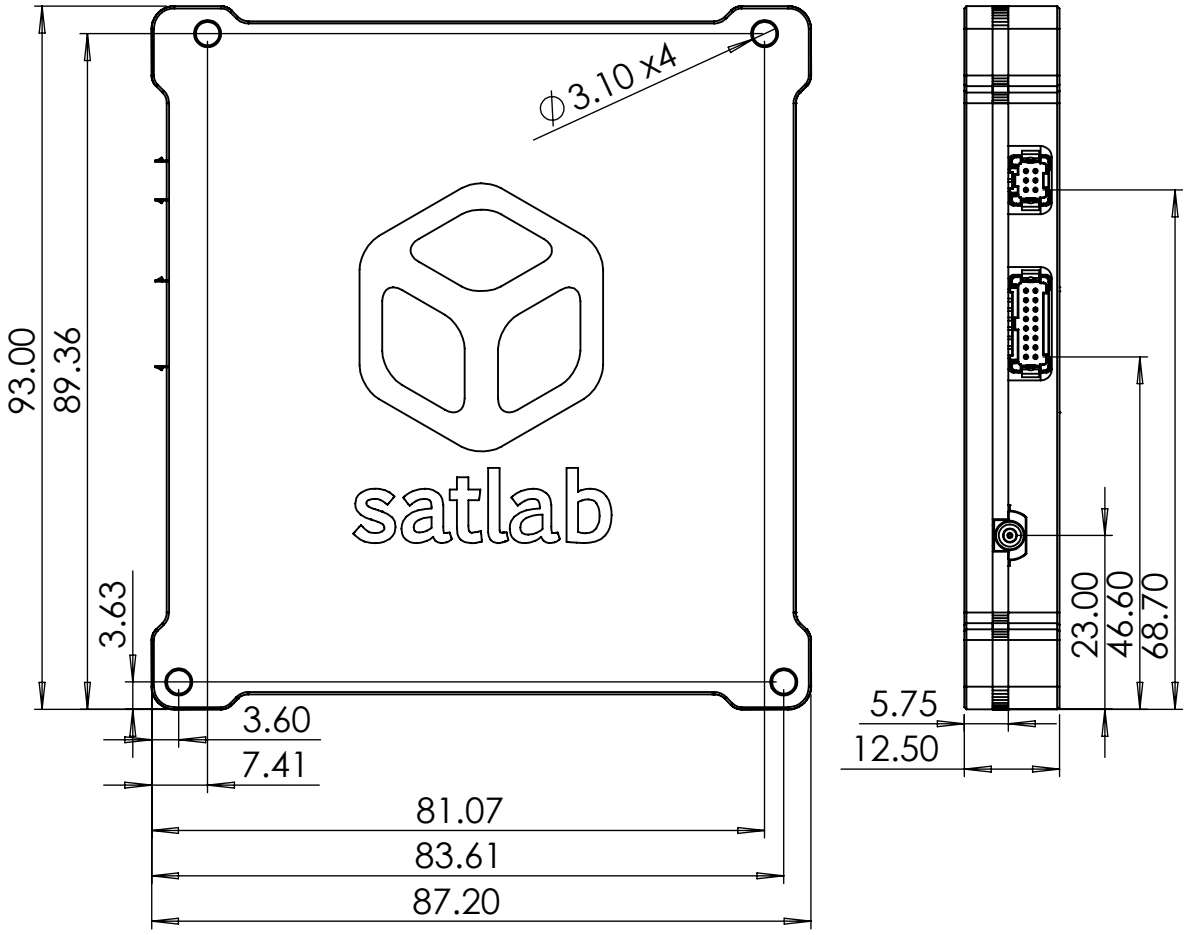


Figure 9: Board outline and side view. All dimensions in mm.

8 Revision History

The document ID of this datasheet is **SLDS-POLARIS-LORA-1.0** and the revision number is **1.0**.

Revision	Date	Description
1.0	2023-09-11	First released version

9 Disclaimer

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